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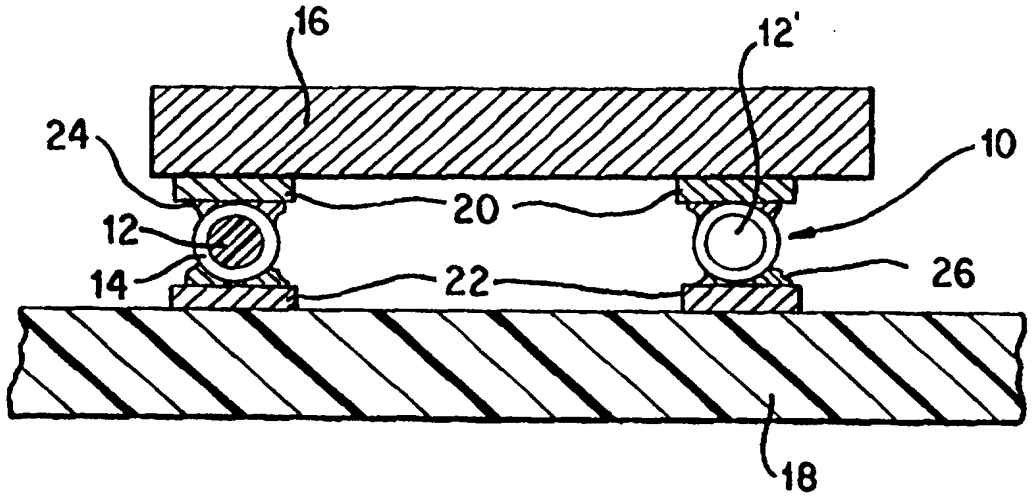


(57) Abstract

An interconnector (10) is provided that improves the reliability of an electrical and mechanical connection between two substrates (16, 18). An interconnector (10) according to the invention includes a compliant core (12) surrounded by an electrically conductive layer (14).

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# IMPROVED SOLDER JOINT RELIABILITY

This invention relates generally to integrated circuits and in particular to providing improved interconnection joint reliability in integrated circuit carriers.

Integrated circuit technology continues to increase semiconductor device density while decreasing device size. Increased semiconductor device density typically leads to increases in device interfaces. Traditional techniques of device packaging cannot effectively accommodate devices with large numbers of interfaces.

One attempt to address large numbers of interfaces include ball grid array (BGA) packages. Conventional BGA packages provide an array of terminal connections on the outside of a device carrier. The device carrier not only provides protection for the device, but also provides connections between the terminal connections and the device. BGA packages provide an improvement over conventional around-the-edge terminal connections in that they can provide a very large increase in the number of available interfaces to the device without increasing device size.

Solder balls, or bumps, or solder columns provide electrical, thermal, and mechanical interconnection between the terminal interconnections of the BGA chip carrier and a substrate. The substrate may be another chip carrier, a printed circuit board, a wafer, or other surface adapted to receive the chip carrier. The solder balls or bumps or columns are formed or placed on either the chip carrier or the substrate

and slightly melted to connect the chip carrier to the substrate.

Flip-chips represent another attempt to address large numbers of device connections. An array of input/output terminals are located on the active surface of a semiconductor device. Solder balls, for example, may be used to interconnect the semiconductor device to a substrate. Solder bumps may also be used.

Typically, the materials in the chip carrier and the substrate or in the device and the substrate differ in coefficients of thermal expansion or are subject to temperature differentials. During thermal cycling which may occur during normal operation, testing, or storage, the interconnection joints, which may be formed by balls or columns, between the chip carrier and the substrate suffer stresses and strains. In some instances, the interconnection joints may break or fracture, thus no longer providing mechanical, thermal, or electrical connection between the chip carrier or device and the substrate.

For example, U.S. Patent No. 5,468,995 issued to Higgins, III provides a columnar electrical connection. The column is a core surrounded by a conductive material. The patent states that solder columns provide benefits over solder balls because columns allow a greater stand-off between the device and the substrate. The columns, however, suffer from temperature cycling fatigue. Thus, Higgins sought to improve the reliability of solder columns by replacing the solder column with a column of a polymeric core surrounded by an outer metallic

coating along the length. Higgins requires, however, that the aspect ratio of the column be greater than 1, that is, its length must be greater than its width to be effective.

Accordingly, there is needed an interconnection joint more able to withstand the stresses and strains suffered when the chip carrier or device and the substrate have differing coefficients of thermal expansion and is easy to use, manipulate, and align.

Accordingly, the present invention is directed to an interconnection joint that substantially obviates one or more of the problems due to limitations and disadvantages of the related art.

In accordance with the purpose of the invention, as embodied and broadly described, the invention, an interconnector for providing electrical, mechanical, and thermal interconnection between a first and second substrate, comprises a core of a compliant material surrounded by an outer layer of an electrically conductive material.

The core is preferably spherical, cylindrical, or cubical in shape. Each shape offers different advantages and features.

In another aspect, the invention provides a method for improving the reliability in an interconnector between a first and a second substrate, by providing a core of a compliant material surrounded by an electrically conductive layer to create an interconnector and affixing the interconnector between the first and second substrates to mechanically, thermally, and electrically interconnect the first and second substrates.

The core may be provided as spherical, cylindrical, or cubical in shape. Each shape offers different advantages and features.

It is to be understood that both the foregoing general description and the following detailed description are exemplary and explanatory and are intended to provide further explanation of the invention as claimed.

The accompanying drawings are included to provide a further understanding of the invention and are incorporated in and constitute a part of this specification, illustrate embodiments of the invention and together with the description, serve to explain the principles of the invention.

In the drawings,

Fig. 1 is a cross section view of a chip carrier or device and a substrate interconnected according to a preferred embodiment of the invention;

Fig. 2 is a cross section of a interconnector according to a preferred embodiment;

Fig. 3 is an illustration of an interconnect column according to another preferred embodiment of the invention;

Fig. 4 is a cross section view of a chip carrier or device and a substrate interconnected using the interconnect column of Fig. 3; and

Fig. 5 is an illustration of a cube interconnector according to the present invention.

An improved interconnect will now be described that improves reliability from coefficient of thermal expansion differences between a chip carrier

or device and a substrate as well as temperature differentials.

Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings.

An exemplary embodiment of the interconnection joints of the present invention is shown in Fig. 1, the joints designated generally by the reference numeral 10. Although illustrated as a sphere, the interconnection joints may be any other suitable shape including, but not limited to, columns or cubes. Of course, each shape offers different advantages and features.

As embodied herein and referring to Fig. 1 spheres 10 include a core 12 and an outer layer 14.

Spheres 10, which replace solder balls or bumps found in conventional packages, electrically, thermally, and mechanically interconnect a first substrate 16 and a second substrate 18. First circuit traces 20 attach to first substrate 16 and second circuit traces 22 attach to second substrate 18. Spheres 10 connect first circuit traces 20 to second circuit traces 22. Solder masses 24 attach spheres 10 to the first circuit traces 20 and solder masses 26 attach spheres 10 to the second circuit traces 22. Solder masses 24 and 26 may be embodied and preferred as a solder or an electrically conductive glue or adhesive.

First substrate 16 may be any type of substrate needing connection to another substrate. For example, in one preferred embodiment first substrate 16 is a BGA package. In a BGA package, circuit

traces 20 provide an electrical connection from the outside of the package to a semiconductor device (not shown) within the BGA package. A BGA package is just one type of first substrate 16. Many other embodiments are equally preferred for first substrate 16 including, flip-chip devices, pad array carriers, chip carriers, discrete devices, and integrated circuit devices.

Second substrate 18 may also be any type of substrate needing connection to another substrate. For example, in one preferred embodiment first substrate 18 is a printed circuit board. In a printed circuit board, circuit traces 22 provide an electrical connection from one point on the board to another. A printed circuit board may contain multiple first substrates 16, described above and connected in a like manner, other types of chip carriers, discrete devices, and interconnection points for electrical components or other printed circuit boards. A printed circuit board is just one type of second substrate 18. Many other substrates are equally preferred including, flip-chip devices, pad array carriers, chip carriers, discrete devices, integrated circuit devices, and other substrates needing a first substrate 16 electrically connected.

Typically, first substrate 16 and second substrate 18 have different coefficients of thermal expansion. Even if they do not, they may experience different thermal cycles. These thermal differences cause first circuit traces 20 and first solder masses 24 to move relative to second circuit traces 22 and second solder masses 26. The movement creates stresses in the interconnect joint. In

conventional solder joints (i.e., solder ball or bumps, or cylinders), these stresses may initiate cracks and allow cracks to propagate through the joint. These cracks may lead to a failure of the interconnect joint. Solder balls or bumps and cylinders are prone to this type of failure because their cores cannot absorb the stresses and strains caused by the differential movement.

The initial aspect ratio for a sphere is approximately 1. Subsequent processing, however, may result in a compressed sphere in which the width is slightly greater than the height.

Spheres 10 according to the present invention, however, do not suffer the same fate. In spheres 10, core 12 is a compliant material that can absorb differential movements caused by thermal coefficient of expansion (TCE) mismatch or differential first and second substrate temperatures.

Preferably, core 12 is a compliant, high temperature polymer, such as polyimide. Equally preferred is a core 12 of a material that can withstand a substrate mounting temperature, be uniform in size, not collapse under substrate weight, and allow a solder or adhesive to adhere to the core. Typically, substrate mounting temperatures are from about 180°C to about 300°C. Preferred materials for core 12 includes rubbers, polyimides, polysulfones, polyetherimides, liquid crystal polymers, other polymers, epoxies, and metals. Core 12 is illustrated as a metal in Fig. 1 by reference 12'. Furthermore, any of the preferred materials for core 12 may preferably include fillers or fibers, an example of which is graphite.

In another equally preferred embodiment, core 12 is a non-compliant fracture resistant material, such as a ceramic. In this embodiment, although a crack may form, it will not propagate as it would in a non-fracture resistant material.

Core 12 is less than about 0.15 inch in diameter. Preferably, core 12 is from about 0.005 inch to about 0.1 inch in diameter. More preferably, core 12 is from about 0.01 inch to about 0.08 inch in diameter. Most preferred, core 12 is from about 0.02 inch to about 0.05 inch in diameter.

An outer, conductive layer 14 surrounds core 12. Outer layer 14 may be any conductive material effective to electrically connect first substrate 16 to second substrate 18. In a preferred embodiment, outer layer 14 is solderable and resistant to oxidation. Solderable and oxidation resistant metals include, for example, lead, tin, silver, nickel, palladium, gold, and alloys thereof. In another preferred embodiment, outer layer 14 is a filled polymer that is electrically conductive, an example of which is a silver-filled epoxy. In another equally preferred embodiment, outer layer 14 may be multiple layers of the preferred materials described above, for example as illustrated in Fig. 2, core 12 may be surrounded by a nickel layer 14a that is surrounded by a silver layer 14b, that is surrounded by a solder layer 14c, or any combination thereof.

Outer layer 14 may be electroless plated, electro-deposited, electroplated, dipped, spray-electroplated, sputtered, chemical vapor deposited (CVD), or evaporated on core 12. Alternatively

preferred, outer layer 14 and/or core 12 may contain materials to enhance adhesion between outer layer 14 and core 12. Alternatively preferred, an additional layer (not shown) may be provided between core 12 and outer layer 14 to improve adhesion between core 12 and outer layer 14.

Each layer in outer layer 14 is from about 1000Å to about 0.01 inch thick. Preferably each layer in outer layer 14 is from about 1000Å to about 0.005 inch thick, more preferably, each layer in outer layer 14 is from about 1000Å to about 0.001 inch thick.

Because core 12 does not easily crack or propagate cracks, cracks that might develop in outer layer 14 would not necessarily create cracks in core 12 or propagate them through core 12 as they would in a metal core. The compliant core 12 absorbs the stresses from TCE mismatch or different thermal first and second substrate temperatures and greatly improves the reliability of the interconnection between first substrate 16 and second substrate 18.

Spheres are more desirable than other shapes because spheres are more easily dealt with in the bonding process. Other shapes require more accurate placement before soldering. But other shapes are alternatively preferred.

For example, another preferred interconnector between substrates 16 and 18 is a cylinder. Cylinders, used similarly to interconnection ball or bumps can offer greater absorption of TCE mismatch stresses and temperature differentials than solder balls or bumps at an equivalent diameter, if their height is greater than their diameter.

In another embodiment, illustrated in Fig. 3, an interconnector is provided in column shape and denoted generally by the reference numeral 30. Interconnector 30 is comprised of a core 32 and an outer layer 34.

Figure 4 illustrates a cross section view of first substrate 16 connected to a second substrate 18 by interconnector 30. Elements from previous preferred embodiments are like numbered.

Core 32 is similar to core 14 except in shape. Core 32 is less than about 0.15 inch in height. Preferably, core 32 is from about 0.005 inch to about 0.1 inch in height. More preferably, core 32 is from about 0.01 inch to about 0.08 inch in height. Most preferred, core 12 is from about 0.02 inch to about 0.05 inch in height.

Except for shape, outer layer 34 is similar to outer layer 14 including materials, thicknesses, and number of layers.

In an alternatively preferred embodiment, an interconnector according to the present invention is a cube as illustrated in Fig. 5 and denoted generally by the reference numeral 36. Cube 36 includes core 38 and outer layer 40.

Core 36 is similar to core 14 except in shape. Core 36 is less than about 0.1 inch in height and width. Preferably, core 36 is from about 0.005 inch to about 0.1 inch in height and width. More preferably, core 36 is from about 0.01 inch to about 0.08 inch in height and width. Most preferred, core 36 is from about 0.02 inch to about 0.05 inch in height and width. The preferred aspect ratio is approximately 1.

Except for shape, outer layer 40 is similar to outer layer 14 including materials, thicknesses, and number of layers.

It will be apparent to those skilled in the art that various modifications and variations can be made in the interconnector of the present invention without departing from the spirit or scope of the invention. For example, other shapes may be envisioned beyond the sphere, cylinder, and cube described herein. Thus, it is intended that the present invention cover the modifications and variations of this invention provided they come within the scope of the appended claims and their equivalents.

WHAT IS CLAIMED IS:

1. An interconnector (10) for providing electrical, mechanical, and thermal interconnection between a first (16) and second (18) substrate, characterized by:

a core (12) of a compliant material; and

an outer layer (14) of an electrically conductive material surrounding the core (12).

2. The interconnector of claim 1 characterized in that the core is spherical in shape.

3. The interconnector of claim 1 characterized in that the width of the interconnector is equal to or greater than a height of the interconnector.

4. The interconnector of claim 1 characterized in that the core is cubical in shape.

5. The interconnector of claim 1 characterized in that the compliant material is selected from the group consisting essentially of rubber and polymers.

6. The interconnector of claim 1 characterized in that the core is polyimide.

7. The interconnector of claim 1 characterized in that the electrically conductive material is selected from the group consisting essentially of silver, nickel, gold, palladium, and alloys thereof.

8. The interconnector of claim 7 characterized in that the outer layer (14) comprises a plurality of layers each being an electrically conductive material.

9. The interconnector of claim 1 characterized in that the compliant material includes a filler or fiber.

10. An interconnector (10) for providing electrical, mechanical, and thermal interconnection between a first (16) and second (18) substrate, characterized by:

a core (12) of a non-compliant fracture resistant material; and

an outer layer (14) of an electrically conductive material surrounding the core (12).

11. The interconnector of claim 10 characterized in that the non-compliant fracture resistant material is a ceramic.

12. A method for improving the reliability in an interconnector (10) between a first (16) and a second (18) substrate, characterized by the steps of:

providing a core (12) of a compliant material;

providing an electrically conductive layer (14) surrounding the core to create an interconnector;

affixing the interconnector (10) between the first (16) and second (18) substrates to mechanically, thermally, and electrically interconnect the first (16) and second (18) substrates.

13. The method of claim 12 characterized in that the step of providing a core (12) includes the step of selecting the compliant material from the group consisting essentially of rubbers and polymers.

14. The method of claim 13 characterized in that the step of providing the electrically conductive layer (14) includes selecting a material for the electrically conductive layer (14) from the group consisting essentially of nickel, gold, palladium, silver, and alloys thereof.

15. The method of claim 12 characterized in that the step of providing the core (12) including the step of providing a width of the interconnector (10) equal to or greater than a height of the interconnector (10).

16. The method of claim 12 characterized in that the step of providing the core (12) including the step of providing the core (12) as cylindrical in shape.

17. The method of claim 12 characterized in that the step of providing the core (12) including the step of providing the core (12) as cubical in shape.

18. The interconnector of claim 12 characterized in that the outer layer (14) comprises a plurality of layers each being an electrically conductive material.

19. The interconnector of claim 12 characterized in that the compliant material is a ceramic.

20. The interconnector of claim 12 characterized in that the compliant material includes a filler or fiber.

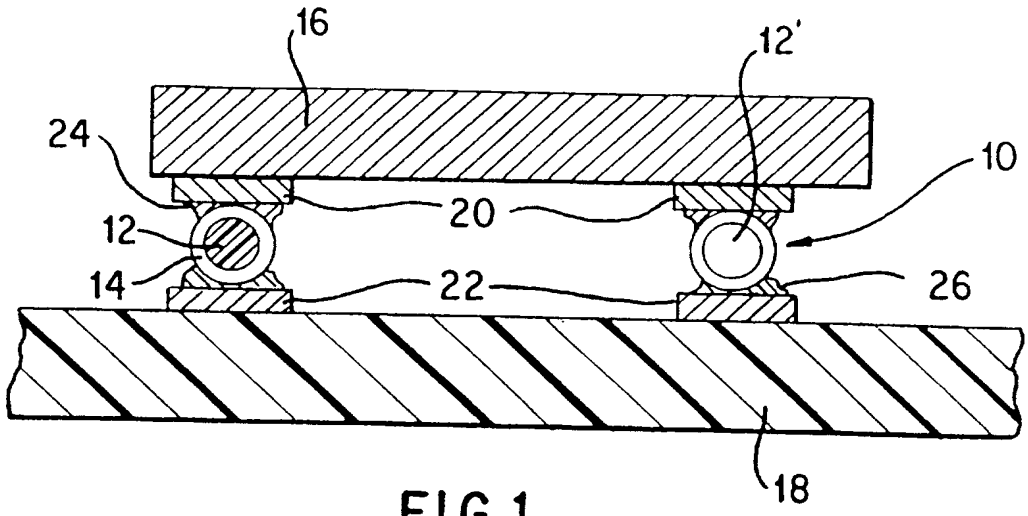


FIG.1

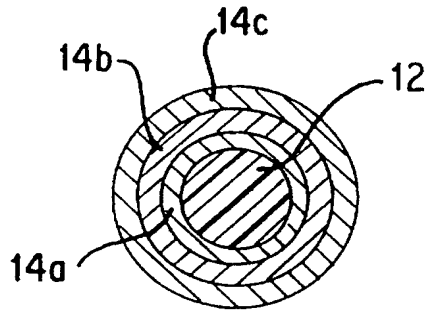


FIG.2

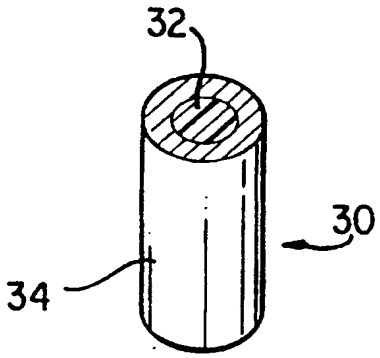


FIG.3

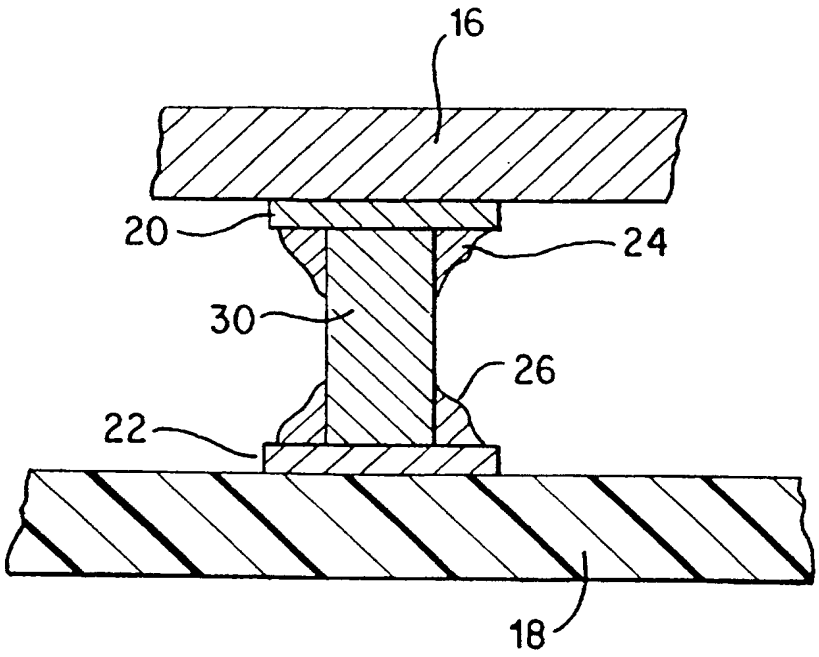


FIG. 4

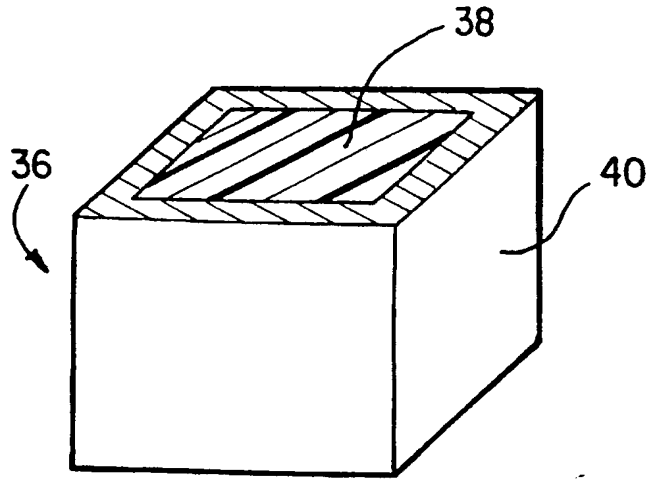


FIG. 5

# INTERNATIONAL SEARCH REPORT

International application No.
PCT/US97/03116

A. CLASSIFICATION OF SUBJECT MATTER
IPC(6) :H01L 23/12
US CL :257/737
According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
U.S. : 257/737, 738, 668,697, 778, 779

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

| Category* | Citation of document, with indication, where appropriate, of the relevant passages | Relevant to claim No. |
|---|---|---|
| X | US 5,235,741A (MASE) 17 August 1993 (17-08-93), Figs.6-7, column 3, lines 12-15, and 21-23. | 1-3,12,14-15. |
| X | JP 02-237129 A (ONO) 19 September 1990 (19-9-90), Figs.1-2, and abstract. | 1-4,12,15, 17 |
| Y | US 5,468,995 A (HIGGINS,III) 21 November 1995 (21-11-95), Fig.2, column 4, lines 21-47, and column 7, lines 39-47. | 5-9,13-14 16,18,20 |
| Y | US 4,807,021 A (OKUMURA) 21 February 1989 (21-02-89), column 4, lines 48-64. | 10-11,19 |

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